presented, and approval and entry are respectfully requested.

REJECTIONS UNDER 35 U.S.C. §101:

On pages 2-3 of the Office Action, the Examiner rejected claims 9-45 under 35 U.S.C. §101 as being directed to nonstatutory subject matter. Applicant respectfully traverses this rejection.

To be patentable, an algorithm must be applied in a "useful" way. See State Street Bank & Trust Co. v. Signature Financial Group, 47 USPQ2d 1596, 1601 (Fed. Cir. 1998). Also, MPEP 2107.01 states that "the Examiner should review the specification to determine if there are any statements asserting that the claimed invention is useful for any particular purpose." Page 1, lines 10-17 of the specification specifies that the present invention relates to a circuit simulation technique for simulating and inspecting a MOS LSI circuit to determine whether "the MOS LSI circuit satisfies design specifications or for improving the performance of the MOS LSI circuit."

Also, page 18, line 35 to page 19, line 5 provides that a circuit to be simulated can be compressed more effectively by integrating a plurality of partial circuits into one circuit, reducing the scale of the circuit to be simulated and allowing simulation of the circuit to be carried out at a high speed. Applicant submits that a method and apparatus for high-speed simulation of an LSI circuit by compressing the LSI circuit to verify design specifications or improve the performance of the circuit are very useful and satisfy the utility requirements.

REJECTION UNDER 35 U.S.C. §112, FIRST PARAGRAPH:

On pages 3-4 of the Office Action, the Examiner rejected claims 9-45 under 35 U.S.C. §112, first paragraph, for the reasons set forth therein. Applicant respectfully traverses this rejection for the reasons presented below.

"Claims are not to be read in a vacuum, and limitations therein are to be interpreted in light of the specification in giving them their 'broadest reasonable interpretation.'" See MPEP 2111.01 and In re Marosi, 218 USPQ 289, 292 (Fed. Cir. 1983). Many of the terms in the claims are described in several different locations of the specification. The cites that follow should be considered as exemplary.

An example of compression and integration is provided in FIGS. 11-13 and the accompanying text of the specification (page 25, line 11 to page 27, line 15). The way simulation is carried out when two or more partial circuits are combined is described on page 27, lines 1-15 of the specification.

Therefore, Applicant respectfully submits that claims 9-45 are patentable and requests reconsideration and withdrawal of the rejections under §112, first paragraph.

REJECTION UNDER 35 U.S.C. §112, SECOND PARAGRAPH:

On pages 5-7 of the Office Action, the Examiner rejected claims 9-45 under 35 U.S.C. §112, second paragraph for the reasons set forth therein. Applicant respectfully traverses this rejection for the reasons presented below.

Applicant again notes that claims must be interpreted in light of the specification, and that the cites to the specification or drawings provided below are exemplary.

Partial circuits are "extracted" based upon the similarities of their corresponding components and terminal connections. See the specification, page 7, lines 1-5; page 17, lines 30-37; and FIGS. 11-13.

The "circuit" is the circuit to be simulated. Page 1, lines 10-17 discloses simulation of MOS LSI circuits.

"Inspection" occurs through comparison of the partial circuits and their components. For example, the configurations of the partial circuits, the operational characteristics of the components of the partial circuits, and the input and output terminals of the partial circuits are

compared. See page 19, line 15 to page 26 of the specification.

An example of "configurations" of the partial circuits are the types of components and their interconnections within the partial circuits. See page 19, lines 21-24.

Partial circuits may "exhibit equivalent operational characteristics" when their corresponding input or output terminals are identical to each other. See page 24, lines 2-11 of the specification and FIG. 9. Equivalence of the partial circuits is determined based upon the configurations of the partial circuits being identical to each other. Thus, for the same input waveform, the output waveforms of the partial circuits are identical to each other.

Partial circuits are "compressed" or reduced in scale through "integration." Partial circuits displaying the same components and terminals or terminal connections are "integrated" or combined into one circuit. See page 3, line 34 to page 4, line 7 of the specification.

"Simulation" is described on page 27, lines 1-15 of the specification. Compression is achieved via integration, then simulation is carried out. Independent claims 9, 21, 33, and 45 have been amended to clarify the order of compression and simulation.

An example of "connectional relationships" of corresponding input and output terminals of two partial circuits is provided on page 5, lines 14-27 of the specification and in FIG. 2(C). In FIG. 2(C), the source of NMOS transistor Q10 of the first partial circuit is connected to a source power supply VSS, while the source of NMOS transistor Q20 of the second partial circuit is connected to the drain of NMOS transistor Q30. The connections differ, thus the two partial circuits are determined not to exhibit the same characteristics. NMOS transistor Q10 of the first partial circuit and NMOS transistor Q20 of the second partial circuit are "corresponding component elements." In this example, the configurations of the partial circuits are not "mutually consistent." See page 17, lines 16-18.

"Intensity of the influence" and "frequency of shifting" are described on page 23, lines 12-25 of the specification and illustrated in FIG. 8. Referring to FIG. 8, if a path is "traced" that "links" external terminal A to terminal E along the route A to Tb to C to Th to E, the intensity of the influence of external terminal A is the frequency of shifting from the source or

drain of the MOS transistor to the gate of the same transistor along the path. When tracing the path from A to E, there is a shift in the source to the gate of Tb and another shift in the source to the gate of Th. Thus, the intensity of influence upon terminal E is 2.

Therefore, Applicant respectfully submits that claims 9-45 are patentable and requests reconsideration and withdrawal of the rejections under §112, second paragraph.

REJECTIONS UNDER 35 U.S.C. §§ 102 AND 103:

The Examiner rejected claims 9-45 under 35 U.S.C. §102(b) as being anticipated by Filseth (U.S. Patent No. 5,473,546). Applicant respectfully traverses this rejection for the reasons presented below.

The Examiner also rejected claims 9-45 under 35 U.S.C. §103(a) as being unpatentable over Shinsha et al. (U.S. Patent No. 4,882,690); or Wang et al., "Restructuring Binary Decision Diagrams Based on Functional Equivalence," IEEE Design Automation, pp. 261-65; or Kuehlmann et al., "Equivalence Checking Using Cuts and Heaps," IEEE Proc. 1997 Design Auto. Conf., pp. 263-68.

Applicant respectfully traverses these rejections for the reasons presented below.

The Invention

The present invention relates to a circuit simulation method and apparatus for simulating and inspecting a large-scale integrated ("LSI") circuit such as a MOS LSI circuit to satisfy design specifications and improve performance of the circuit. Because a MOS LSI circuit is large in scale, the circuit needs to be simplified while ensuring accuracy of circuit operation. Simplifying the circuit reduces the time required for simulation and enables high-speed simulation.

In one embodiment of the present invention, first, partial circuits are extracted from the circuit to be simulated. The partial circuits are inspected for equivalence. If the

configurations of the partial circuits are consistent with each other, then the operational characteristics of the corresponding circuit elements are compared with each other. Next, if all pairs of corresponding circuit elements have the same operational characteristics, then the input and output terminals are compared with each other. If the corresponding input and output terminals are identical, then the operational characteristics of the partial circuits are considered to be equivalent. However, if the input or output terminals are not identical, then the partial circuits connected to the input or output terminals are inspected for quasi-equivalence. If the input or output terminals are quasi-equivalent circuits, the partial circuits are considered to be equivalent.

To distinguish partial circuits, the intensity of the influence of an external terminal of the extracted partial circuits upon the extracted partial circuits is taken into account. The intensity of the influence of the external terminal is assessed as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof in the course of tracing a path linking the external terminals and an object terminal. Even if the connected states of corresponding external terminals of two partial circuits are mutually inconsistent, as long as the intensities of currents flowing from the external terminals placed in the inconsistent connected states are equal to or larger than a designated value, the influence of the external terminals is considered to be negligible. Consequently, the partial circuits are judged to exhibit equivalent operational characteristics.

After the circuit is compressed by integrating the partial circuits exhibiting the equivalent operational characteristics into one circuit, circuit simulation is carried out.

In conventional circuit simulation methods, only circuit elements located in a limited area within a circuit can be inspected to determine if they exhibit the same characteristics. It is difficult to distinguish all circuit elements exhibiting equivalent operational characteristics in the circuit. Thus, the circuit is not compressed effectively. In contrast, in the present invention, integrating a plurality of partial circuits into one circuit can be readily achieved. As a result, a circuit to be simulated can be compressed more effectively, reducing the scale of the

circuit.

The References

Filseth. Filseth relates to expanding or flattening hierarchical design descriptions using a "linker" or "flattener." The output from a linker is a flattened or expanded description of the input circuit descriptions. In Filseth, copies are created of submodule descriptions that are used more than once. This creates a flattened representation of the input hierarchical design, typically in the form of a tree structure. See Filseth, col. 1, lines 6-7; col. 2, lines 1-2; and col. 3, lines 18-29.

Shinsha et al. Shinsha relates to a method for automatically updating gate-level logic in response to altering functional-level logic. See Shinsha, abstract.

Wang et al. Wang relates to a method for restructuring a binary decision diagram (BDD) from a given input ordering to any other ordering, based on functional equivalence and the BDD's structure equivalence. See Wang, abstract.

Kuehlmann et al. Kuehlmann relates to comparing large combinational circuits with some structural similarities. See Kuehlmann, abstract.

The Present Claimed Invention Distinguishes Over the Prior Art

Claim 9 of the present invention specifies extracting a plurality of partial circuits, inspecting the partial circuits to detect partial circuits exhibiting equivalent operational characteristics, and integrating the partial circuits exhibiting equivalent operational characteristics into one circuit.

Filseth discloses a method for flattening hierarchical descriptions of electronic circuits using a program called a "linker" or "flattener." In Filseth, complex logic circuit descriptions represented hierarchically are expanded into flat circuit descriptions for circuit simulation. In other words, the program "linker" or "flattener" reads hierarchical descriptions of electronic circuits and produces flat circuit descriptions that are larger in circuit size than the hierarchical

descriptions. Filseth presumes that hierarchical descriptions of electronic circuits cannot be used to perform circuit simulation, and that simulation is performed only by using flat logic circuits represented by the enlarged flat circuit descriptions. In contrast, the present invention performs circuit simulation by integrating partial circuits exhibiting equivalent operational characteristics into one circuit, resulting in compression of the circuit to be simulated.

Thus, Filseth is directed to a different technology and teaches techniques to solve a different goal and problem than the present invention. The time required for performing circuit simulation in Filseth using flat logic circuits increases because the circuit size of the flat logic circuits increases. Consequently, dealing with LSI circuits using the method of Filseth becomes very difficult. In contrast, the time required for performing circuit simulation in the present invention is reduced because the size of the circuit to be simulated is reduced by integrating partial circuits into one circuit.

Shinsha discloses a method that automatically updates gate-level logic according to modifications of functional-level logic. In Shinsha, when the new gate-level logic is produced by altering the functional-level logic, the new, altered gate-level logic is compared with the current, unaltered gate-level logic. Corresponding and non-corresponding portions are determined and extracted. Corresponding portions (i.e., sublogics) are portions logically common to the new and current gate-level logic. The gate-level logic is updated using current physical design information obtained for the current gate-level logic for the corresponding portions, and also using new physical design information obtained for the non-corresponding portions. The updated gate-level logic is produced by coupling the corresponding portions that do not need to be modified with the non-corresponding portions that have been modified using the new physical design information.

In contrast, the present invention determines whether partial circuits extracted from the circuit to be simulated exhibit equivalent operational characteristics. Before circuit simulation is performed, the circuit is compressed by integrating the partial circuits exhibiting equivalent operational characteristics into one circuit.

Also, in Shinsha, the corresponding portions common to the new gate-level logic and the current gate-level logic are determined on the basis of functional-level logic. In contrast, the present invention determines whether the extracted partial circuits exhibit equivalent operational characteristics based upon configurations of the partial circuits (e.g., components of the partial circuits and the connectional relationships between the components).

Furthermore, Shinsha has a disadvantage in that two sublogics having different delay characteristics may be determined to be common to one another. Although two types of sublogics may have the same functional-level logic, the delay time of signals that are transferred in one of these sublogics may be different from that in the other sublogic if the circuit configurations of the sublogics are different. Consequently, it is not possible to use the method of Shinsha to perform circuit simulation by integrating partial circuits (sublogics) exhibiting equivalent operational characteristics into one partial circuit.

Wang relates to a method for restructuring a binary decision diagram (BDD) from a given input ordering to any other ordering, based on functional equivalence and the BDD's structure equivalence. Kuehlmann discloses a method for checking functional equivalence of combinational circuits.

Similar to Shinsha, both Wang and Kuehlmann search for common portions of different types of BDDs or combinational circuits based upon functional-level logic. Consequently, is not possible to use the methods of Wang and Kuehlmann to perform circuit simulation by integrating partial circuits (BDDs or combinational circuits) exhibiting equivalent operational characteristics into one partial circuit.

Similar to claim 9, independent claims 21, 33, and 45 also specify extracting a plurality of partial circuits, inspecting the partial circuits to detect partial circuits exhibiting equivalent operational characteristics, and integrating the partial circuits exhibiting equivalent operational characteristics into one circuit. Thus, for the reasons presented above with respect to claim 9, it is submitted that independent claims 9, 21, 33, and 45 patentably distinguish over the prior art. Accordingly, Applicants respectfully request reconsideration and withdrawal of the

rejections under §§ 102 and 103.

As for the dependent claims, the dependent claims depend from the above-discussed independent claims and are patentable over the prior art for the reasons discussed above. The dependent claims also recite additional features not taught or suggested by the prior art. For example, claim 18 recites "assessing the intensity of influence of an external terminal is determined as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking the external terminal and a given terminal of each of the plurality of partial circuits." Therefore, for at least this reason and the reasons set forth above with respect to the independent claims, it is submitted that the dependent claims patentably distinguish over the prior art.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding rejections, the application is submitted to be in condition for allowance, which action is earnestly solicited. At a minimum, this Amendment should be entered at least for purposes of Appeal because it either clarifies and/or narrows the issues for consideration by the Board.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 11/21/00

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